

Abstract

In recent years, the demand for efficient and reliable communication networks has greatly increased. To satisfy this need, powerful error correcting codes were introduced. The (iterative) algorithms used for decoding such modern codes are computationally very demanding and need great computing power to deliver real-time results. Mobile users, however, ask for low-power electronics; the combination of both demands led to an increased interest in analog communication circuits, e.g., in analog decoders for error correcting codes.

The first part of this thesis discusses various implementations of analog decoders. An analog decoder can be understood as a code-representing (factor) graph mapped on analog silicon, whereas the decoding algorithm (e.g., the sum-product algorithm) corresponds to the settling behavior of the analog circuit. The performance gain of analog decoders compared to digital implementations in terms of speed or power-consumption is believed to be at least a factor of 100.

The following implementations of such analog decoders are discussed: Hamming decoders built out of two generations of discrete softgates, an integrated Hamming decoder and an integrated Reed-Muller decoder are presented. An extensive collection of measured error-rate curves of all decoders under various operating conditions prove their full functionality and demonstrate their behavior under transistor mismatch.

Furthermore, a novel circuit to compute the soft symbols for a PAM or QAM signal is presented. This simple transistor network blends in nicely with analog decoders—its outputs are currents proportional to the symbol-likelihoods.

The second part of this thesis is devoted to analog-to-digital and digital-to-analog converters with minimal-sized elements. Digital data processing is pervasive, and the need for fast, high-resolution and low-power converters persistent. Highly accurate converters usually require large elements to achieve the desired minimal mismatch; large elements however demand high currents for high speed. This trade-off can be circumvented by using small-sized, yet imprecise, elements and then adding digital post-correction circuitry.

It can be shown, that the effective resolution of a digitally-corrected analog-to-digital converter only weakly depends on the comparator mismatch. Therefore, such converters can be built with minimal-sized elements and a digital post-correction. This was confirmed by measurements on an integrated flash analog-to-digital converter containing 256 low-precision comparators and achieving an effective resolution of nearly 7 bits.

A similar statement holds for current-steering digital-to-analog converters with almost minimal-sized current sources: for a converter containing 12 low-precision current sources and digital pre-correction, an effective resolution of more than 10 bits was achieved—virtually irrespective of the mismatch.

The thesis is concluded by a summary of the obtained results and a collection of research proposals in the field of analog decoding and for digitally-corrected converters.

Keywords: Factor graphs, message-passing algorithms, sum-product algorithm, analog non-linear transistor circuits, translinear circuits, analog iterative decoders, soft symbol detection, digital data transmission, analog-to-digital converter, digital-to-analog converter, calibration, post-correction, imprecise elements.