Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

On Analog Decoders and Digitally Corrected Converters

Matthias Frey

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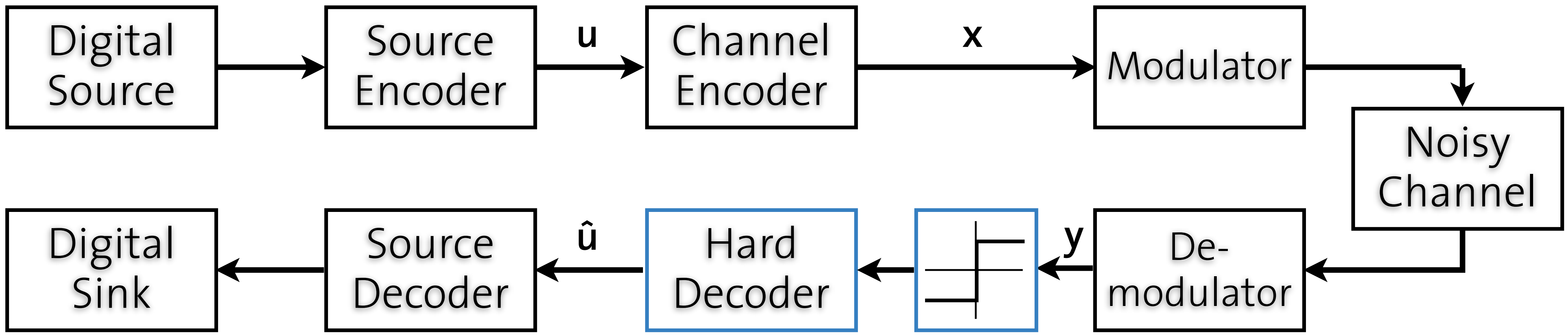
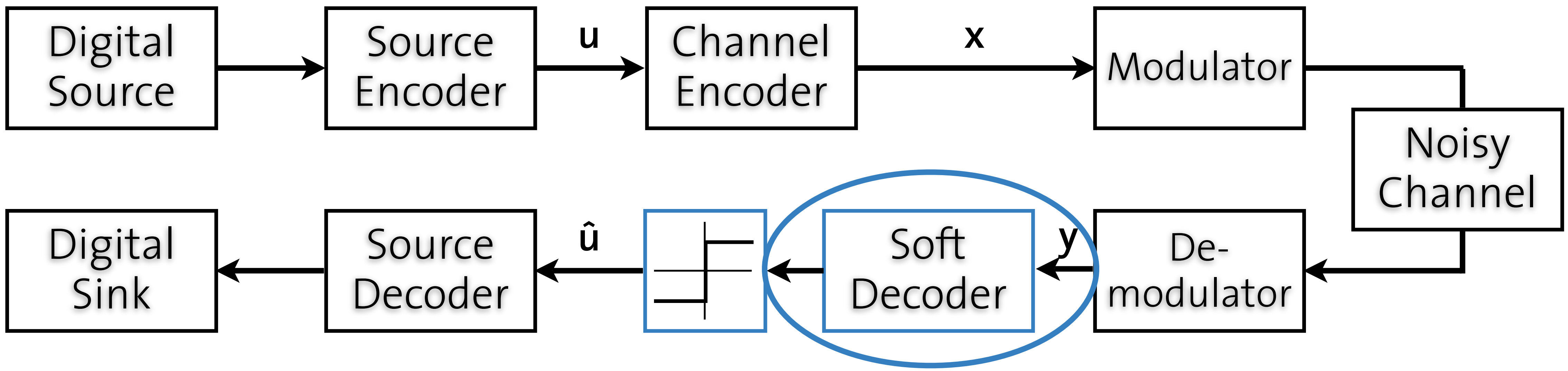
Introduction to Analog Decoding

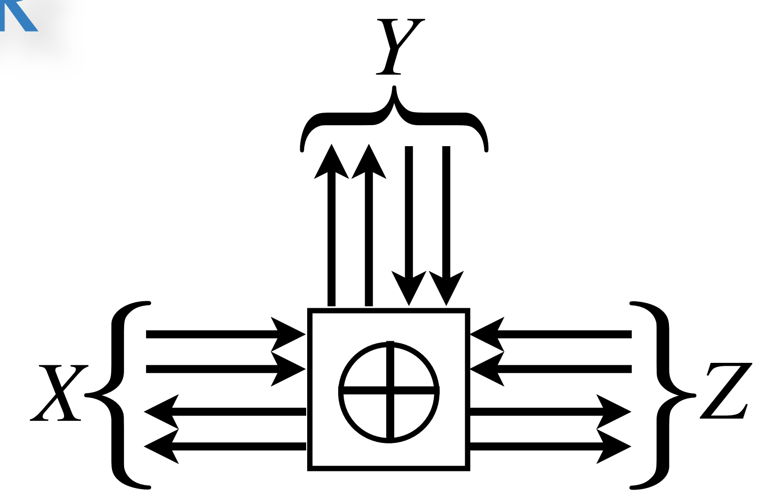


Soft Decoder has probabilities as inputs (instead of bits);
this soft-information enhances the performance of the decoder.



Softgates vs. Logic Gates

Example: SoftXOR



$$x \oplus y = z$$

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

Analog Decoding:

$$\frac{I_{Z=0}}{I_{Z=0} + I_{Z=1}} = p(Z = 0)$$

Probabilities are represented by currents

$$p_{Z\text{out}}(0) = p_{X\text{in}}(0) \cdot p_{Y\text{in}}(0) + p_{X\text{in}}(1) \cdot p_{Y\text{in}}(1)$$

$$p_{Z\text{out}}(1) = p_{X\text{in}}(0) \cdot p_{Y\text{in}}(1) + p_{X\text{in}}(1) \cdot p_{Y\text{in}}(0)$$

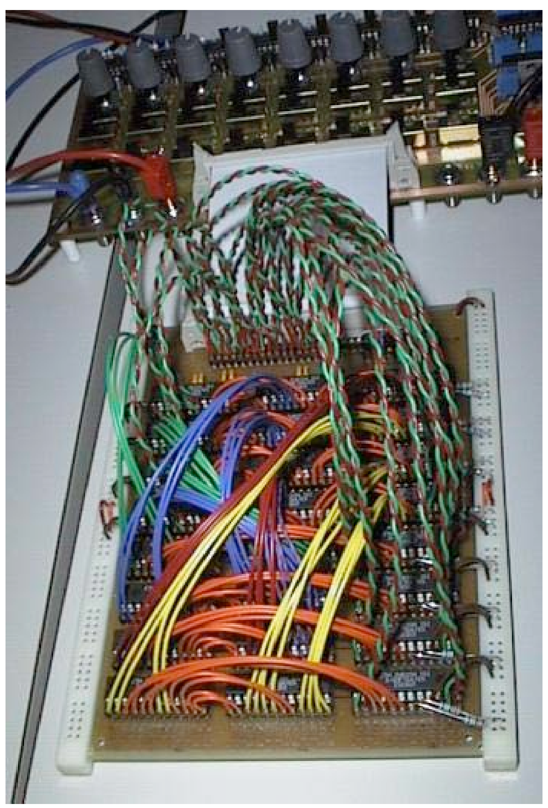
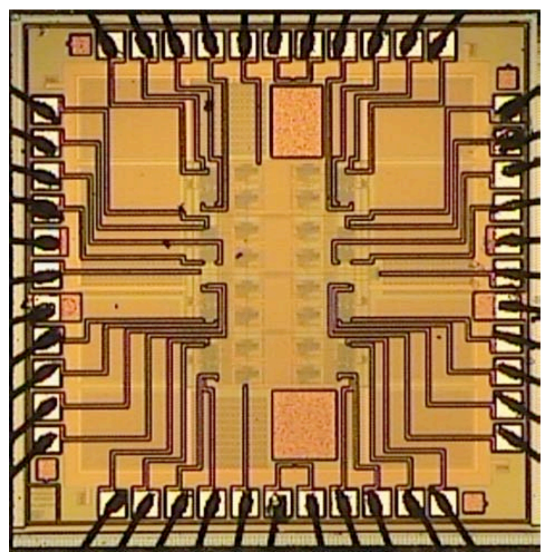
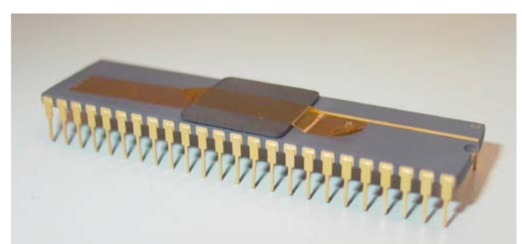
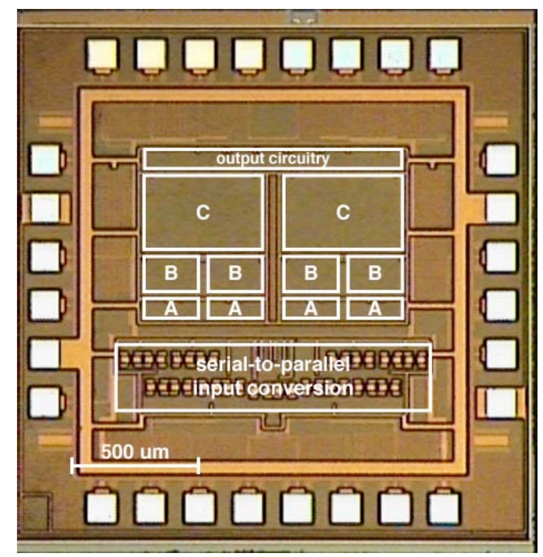
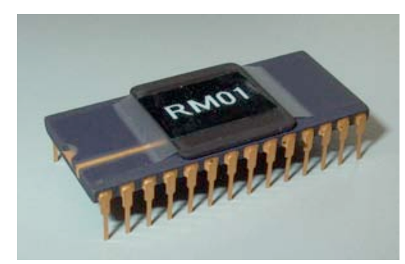
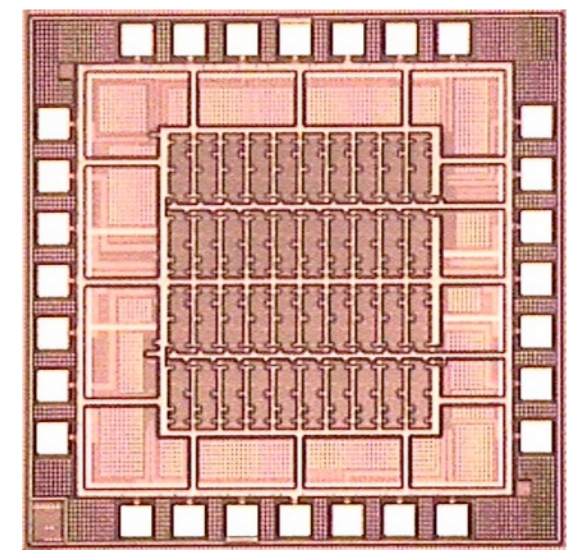
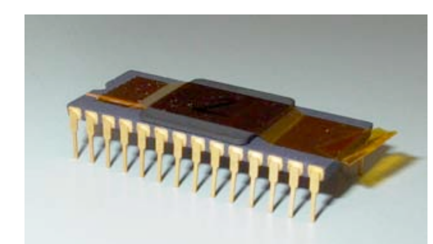
$$\frac{I_{Z=1}}{I_{Z=0} + I_{Z=1}} = p(Z = 1)$$

analog current multiplication

analog current summation

Softgates can easily be implemented with simple analog circuits

Examples of Analog Decoders

2001-2002	January 2003	May 2004	September 2005
	 	 	 
Discrete Hamming Decoder	(8,4,4) Hamming Decoder Chip	(16,5,8) Reed-Muller Decoder Chip	Analog Coprocessor Chip

chip fabrication was funded
by IBM Research, Zürich, Switzerland

Comments on the Measurements

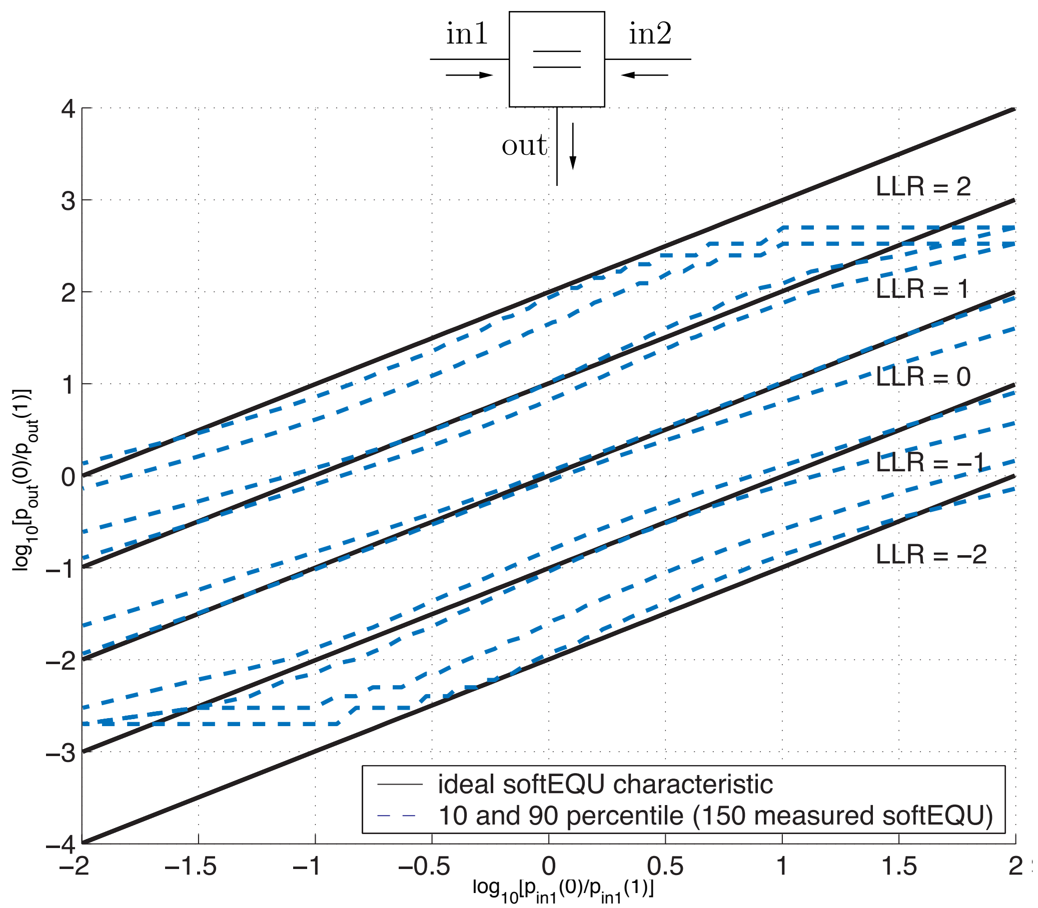
- Analog Decoders are **robust**, but not entirely immune to **transistor-mismatch**.
- The **performance** of the decoder depends on the **decoding time**; the bit-error rate depends on the desired performance.
- The error-correction capability may **improve** with an increased current level, by moving **from weak to moderate inversion**.
- Analog Decoders (in subthreshold CMOS) can be operated at **low supply voltages** and at **very low power** levels.

Measurements:

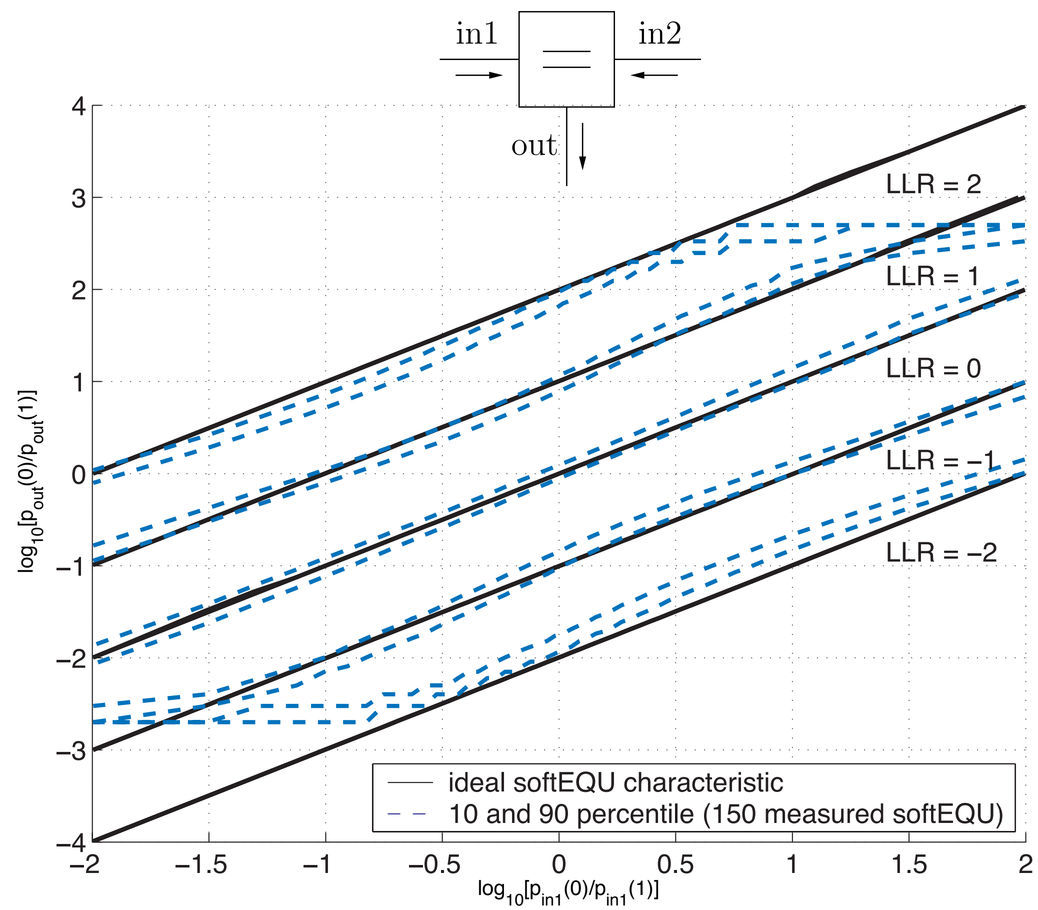
Effects of Non-Idealities on Softgate-Characteristics

- Scattering of 150 measured gate characteristics

1st Generation Softgates



2nd Generation Softgates



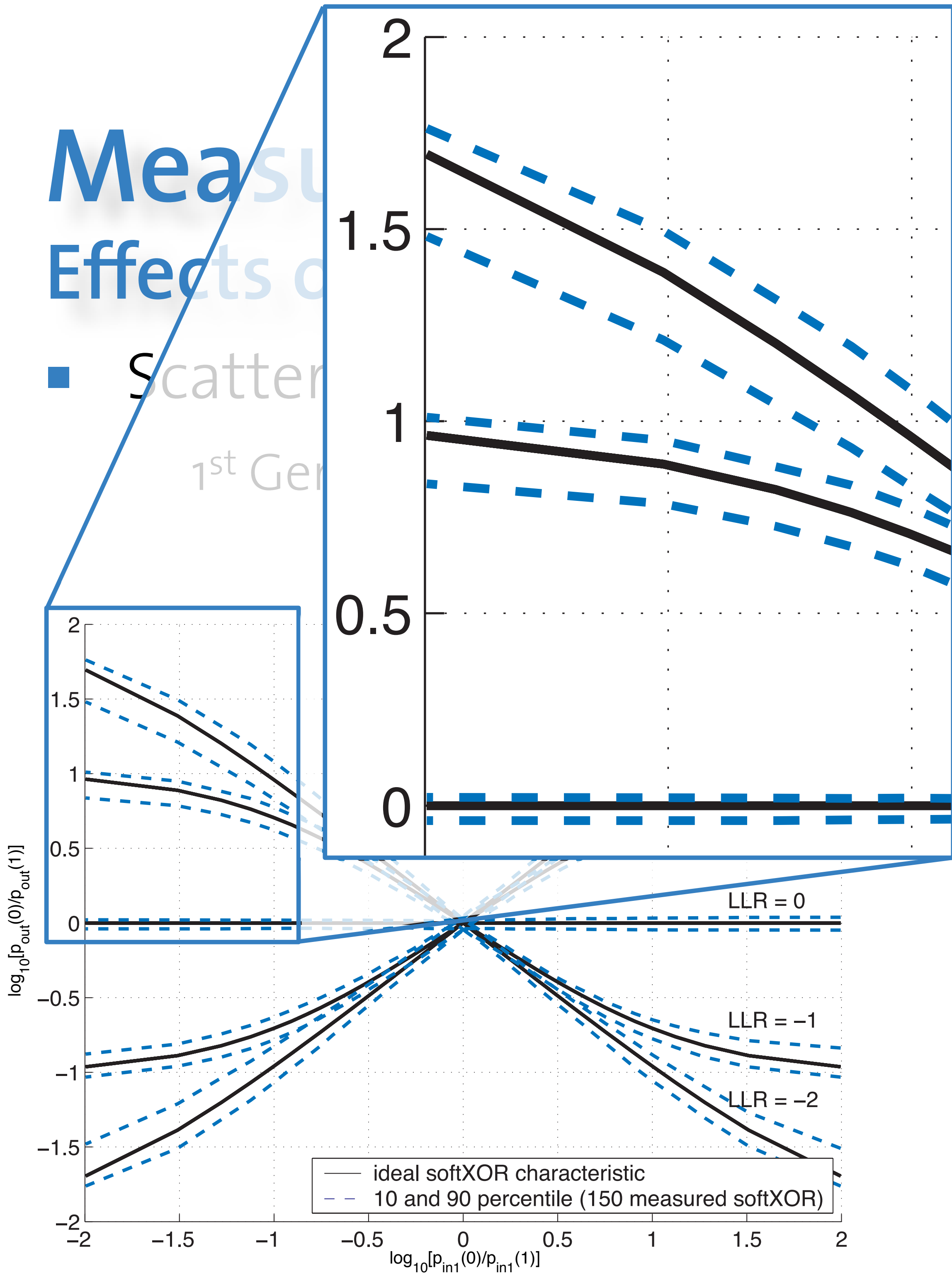
in1: x-Axis, in2: parameter, out: y-Axis. all values represented as LLRs: log(p(0)/p(1))

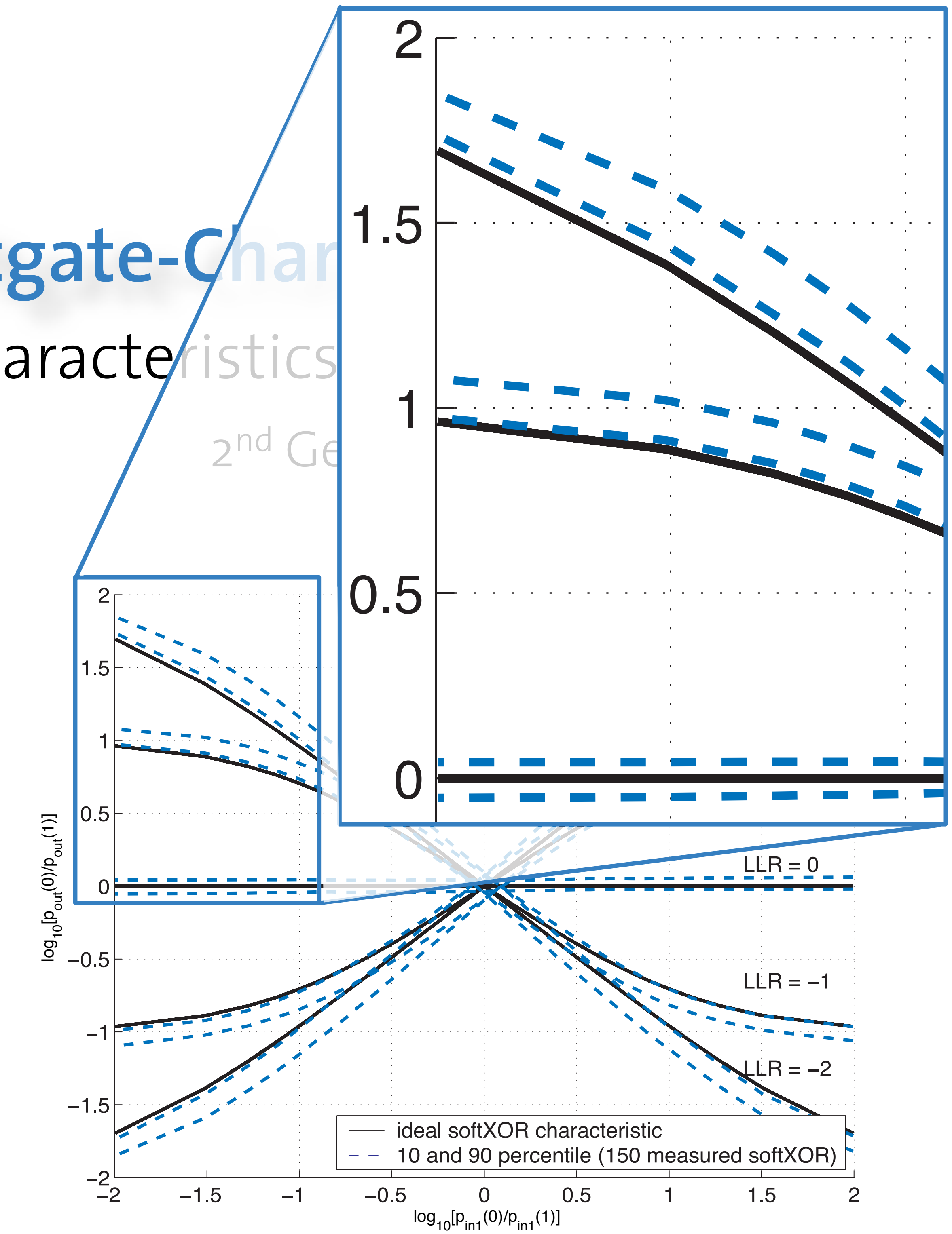
Mea

Effects o… n Softgate-Char…

- Scatter… ate characteristics

1st Ge… 2nd Ge…



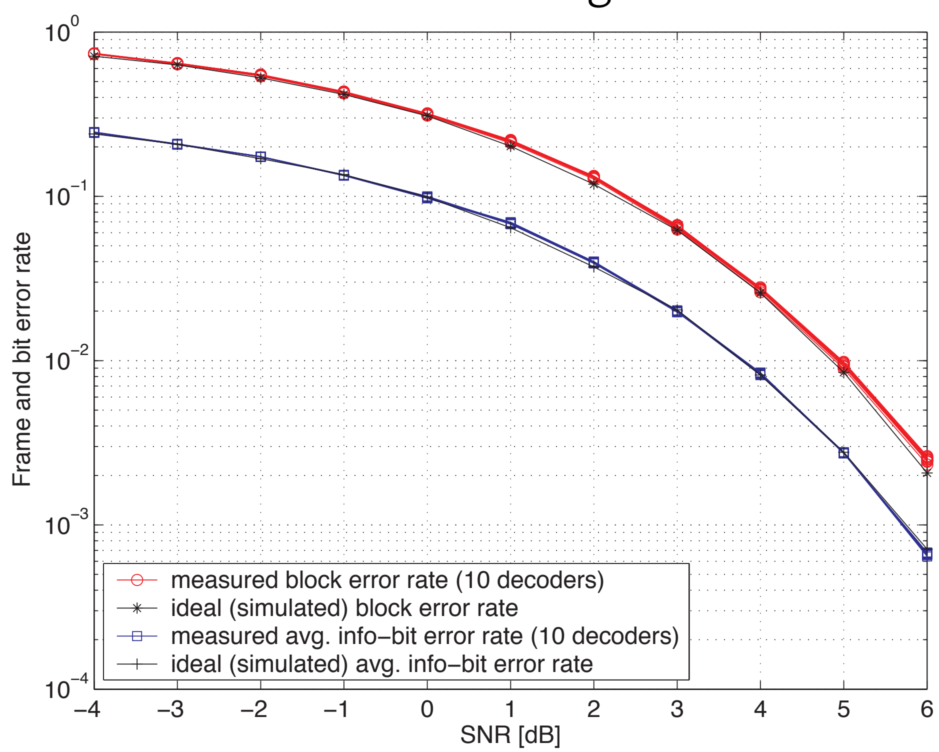


in1: x-Axis, in2: parameter, out: y-Axis. all values represented as LLRs: log(p(0)/p(1))

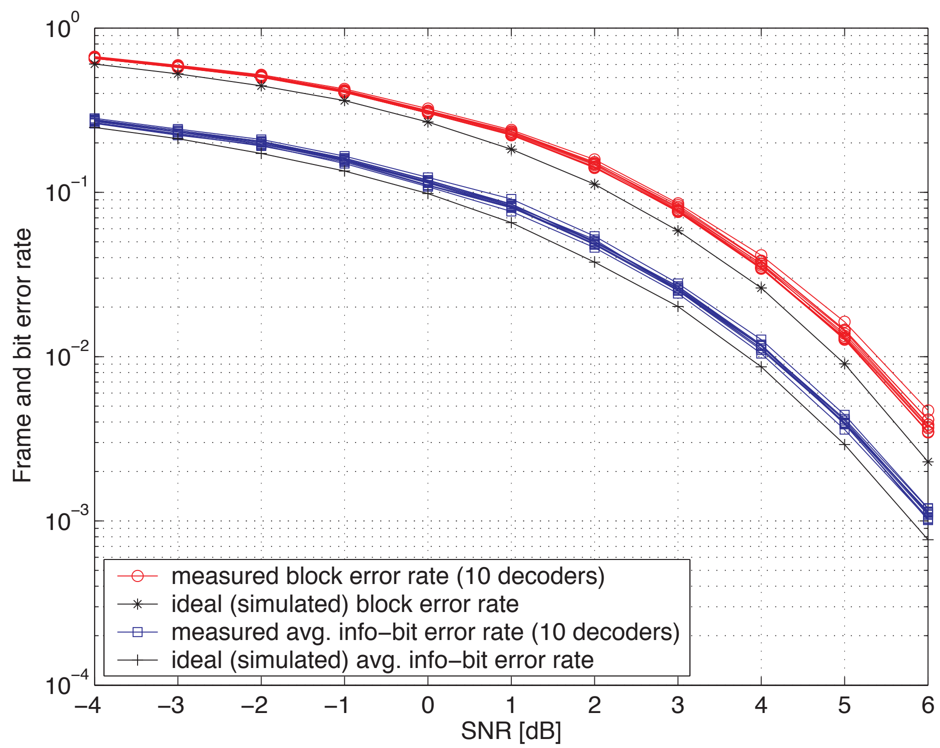
Measurements:

Effects of Non-Idealities on Error Rate Curves

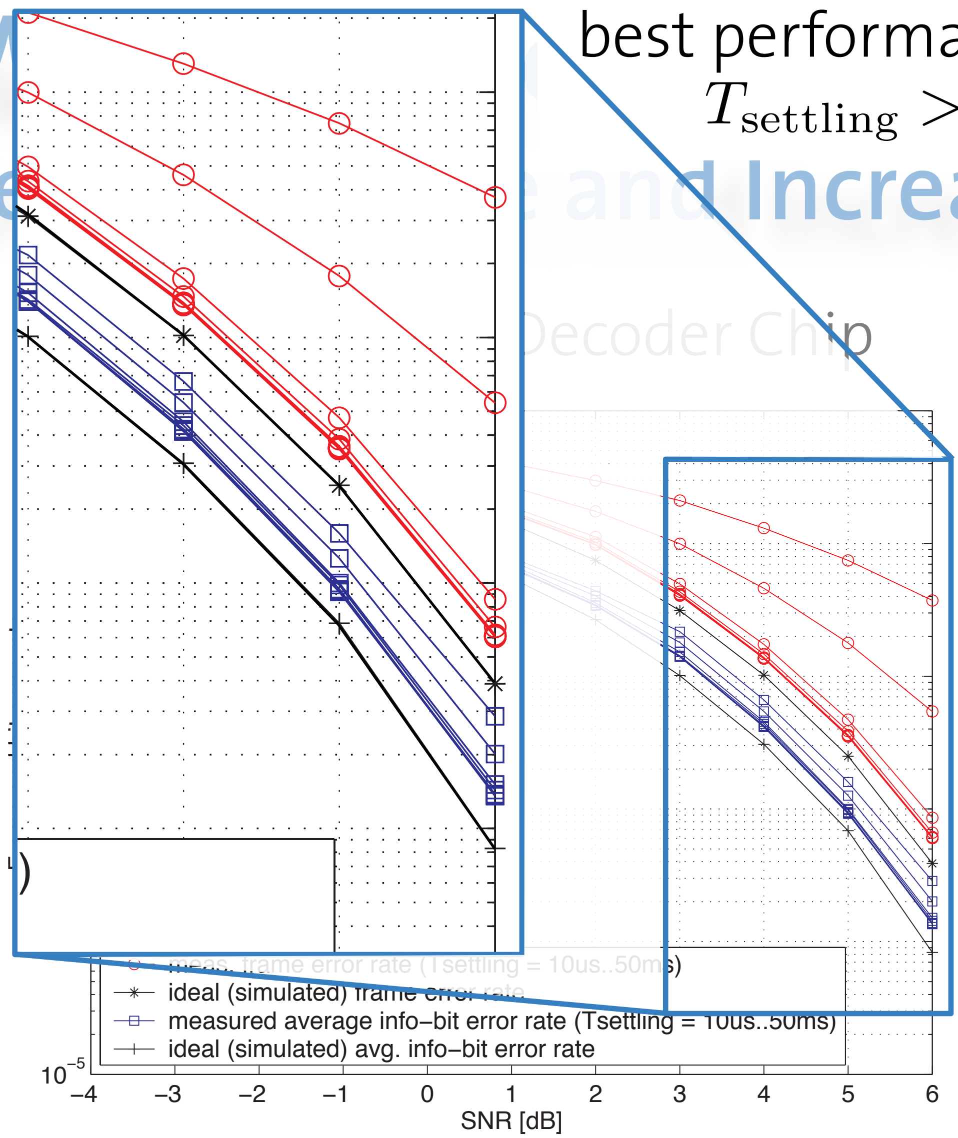
1st-Generation
Discrete Hamming Decoder



2nd-Generation
Discrete Hamming Decoder

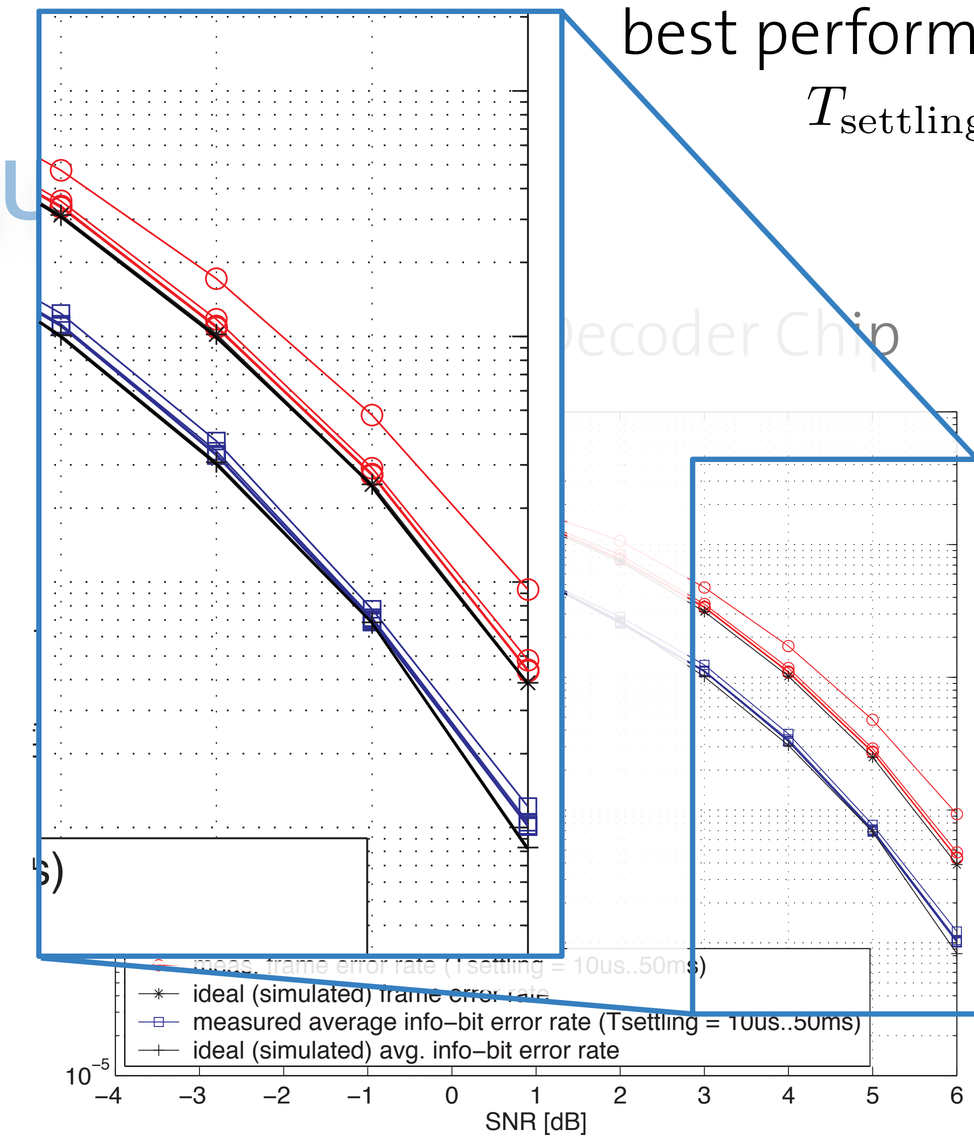


- Analog Decoders are **robust**, but not entirely immune to **transistor mismatch**.



best performance for
$T_{\text{settling}} > 100\ \mu s$

(nominal unit current)



best performance for
$T_{\text{settling}} \geq 20\ \mu s$

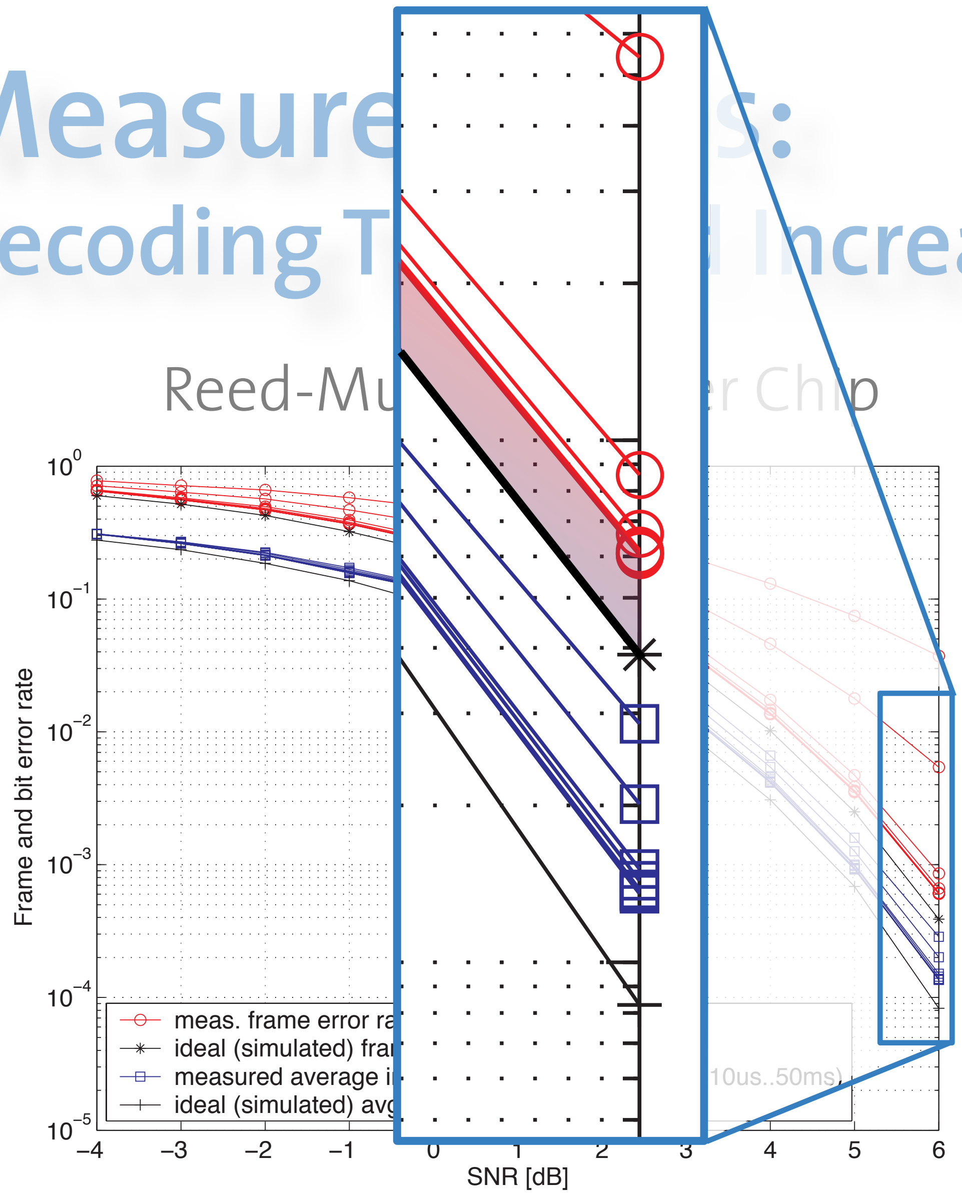
(30x nominal unit current)

- The **performance** of the decoder depends on the **decoding time**; the bit-error rate depends on the desired performance.

Measure...s:

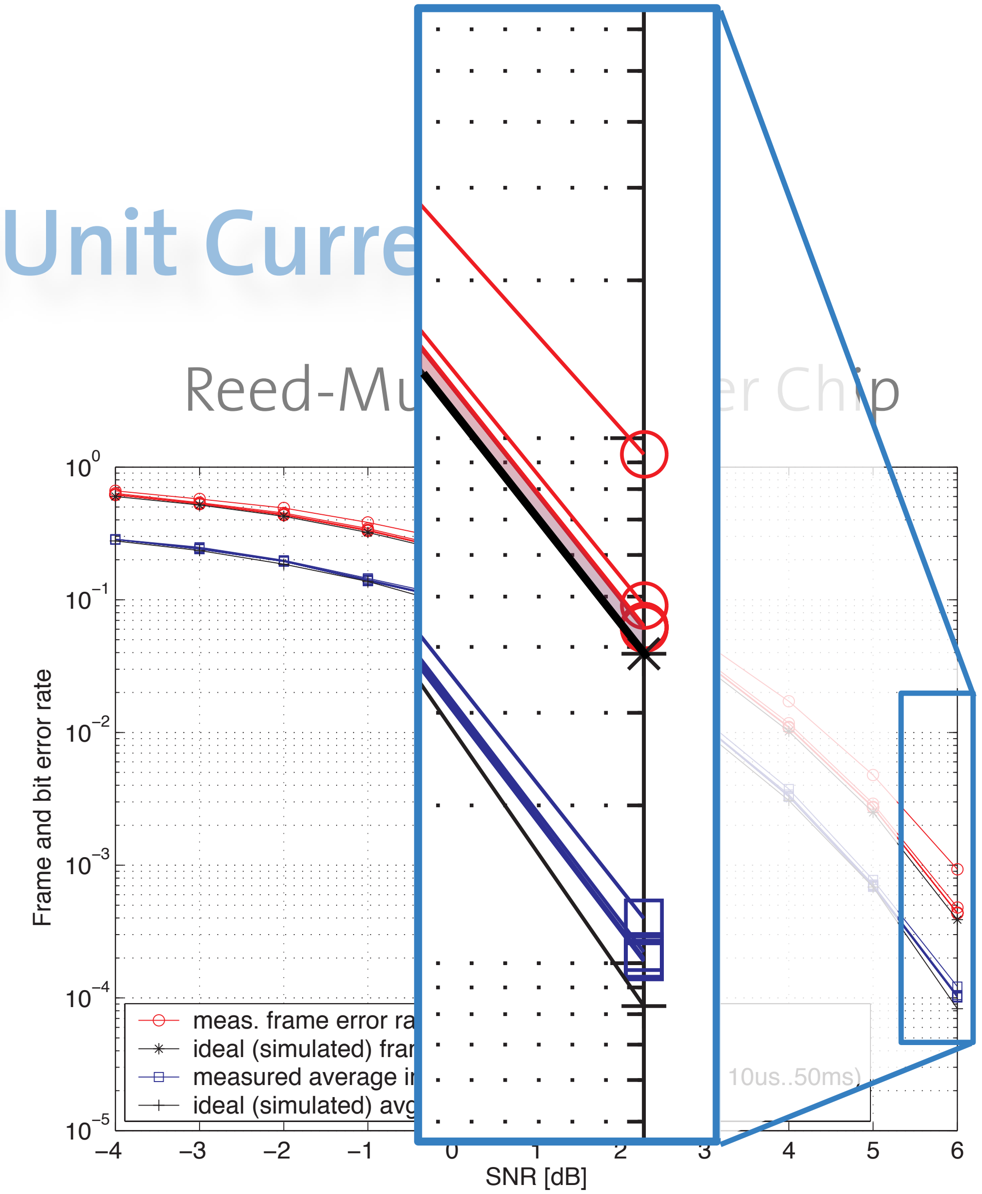
Decoding T... Increased Unit Curre...

Reed-Mu... Chip



(nominal unit current)

Reed-Mu... Chip

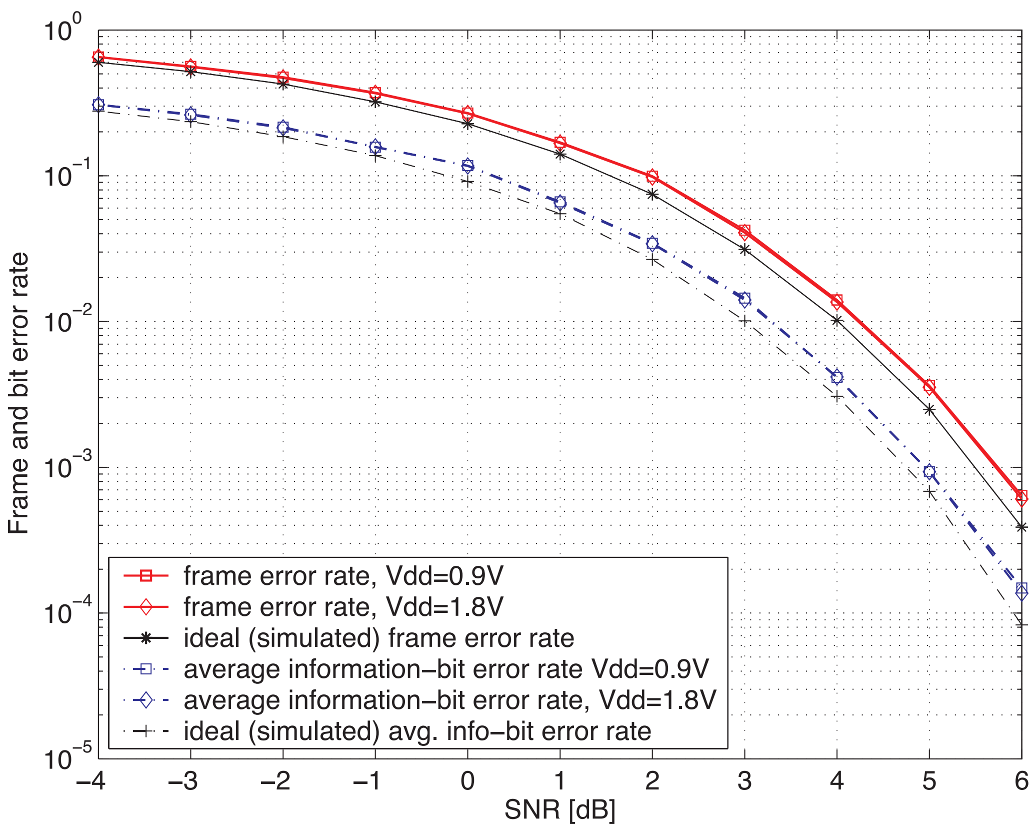


(30x nominal unit current)

- The error-correction capability may **improve** with an increased current level, by moving **from weak to moderate inversion**.

Measurements:
Minimal Supply Voltage

Integrated Reed-Muller Decoder
(nominal unit current)



- Hamming Decoder:
  - min. Vdd = 0.7 V (nom. Vdd = 1.8 V)
  - Average power dissipation ≈ 50 μW
  - Energy per decoded info-bit = 150 nJ
- Reed Muller Decoder:
  - min. Vdd = 0.9 V (nom. Vdd = 1.8 V)
  - Average power dissipation ≈ 50 μW
  - Energy per decoded info-bit = 11 nJ

- Analog Decoders (in subthreshold CMOS) can be operated at **low supply voltages** and at **very low power** levels.

Conclusions, Outlook

- 2 generations of softgates and 2 analog decoder ASICs were implemented successfully.
- Various measurements prove the decoders' functionality under different operating conditions.

- Different approaches for analog decoders are possible:
  - reprogrammable mixed signal ASIC (analog coprocessor)
  - low-power decoder (biomedical applications, sensor networks, etc.)
  - high-speed decoder (10Gbit-Ethernet, data-links, etc.)

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- ➡ **Digitally-Corrected A/D- and D/A-Converters**
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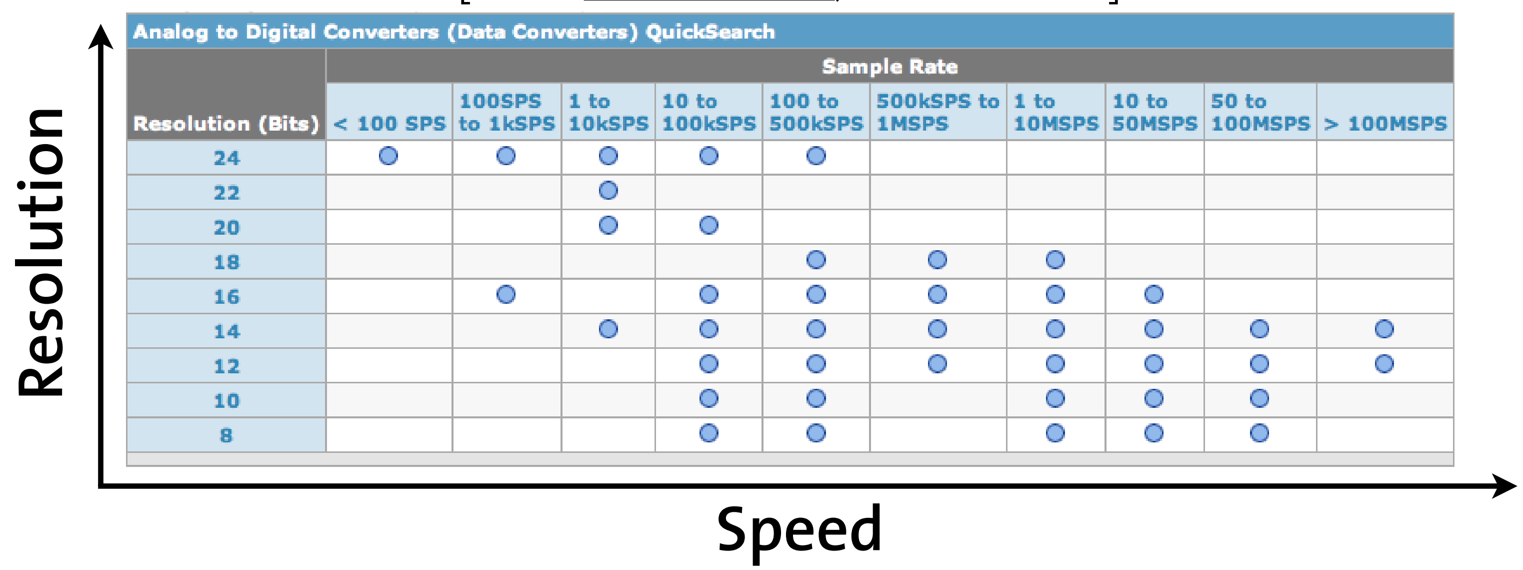
Digitally Corrected Converters

Motivation:

[from www.ti.com, March 2006]



Analog to Digital Converters (Data Converters) QuickSearch

Resolution (Bits)	Sample Rate									
	< 100 SPS	100SPS to 1kSPS	1 to 10kSPS	10 to 100kSPS	100 to 500kSPS	500kSPS to 1MSPS	1 to 10MSPS	10 to 50MSPS	50 to 100MSPS	> 100MSPS
24	●	●	●	●	●					
22			●							
20			●	●						
18					●	●	●			
16		●		●	●	●	●	●		
14			●	●	●	●	●	●	●	●
12				●	●	●	●	●	●	●
10				●	●		●	●	●	
8				●	●		●	●	●	

Trade-off between resolution and speed!

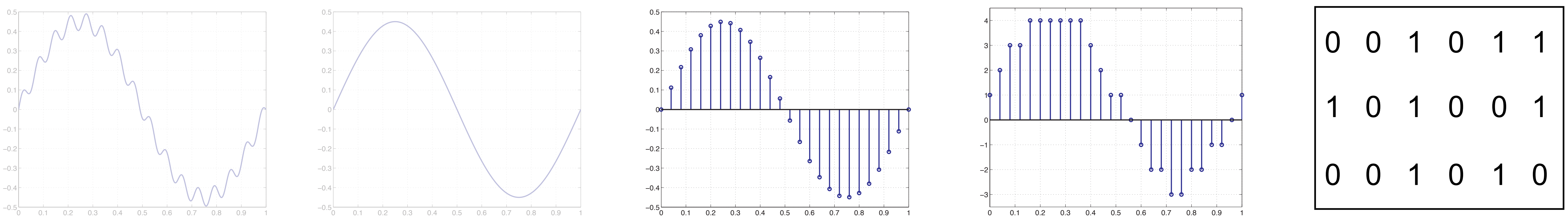
high resolution ⇔ small device mismatch ⇔ large devices

high speed ⇔ small devices

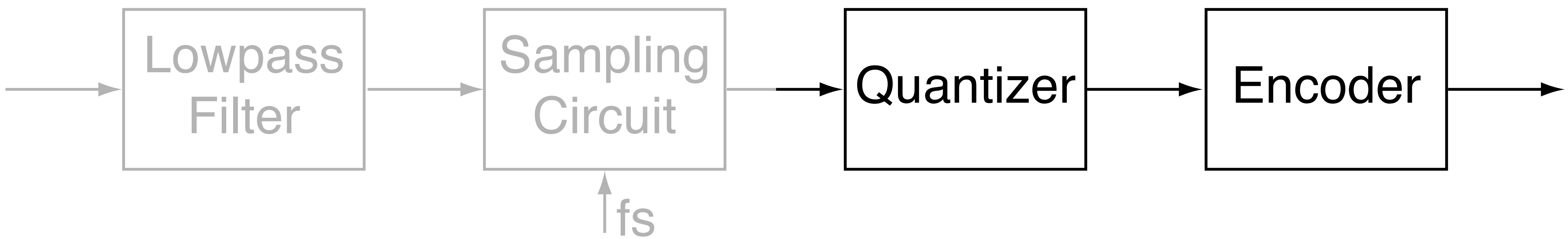
⇒ small and imprecise devices + digital correction

(instead of large and precise devices)

Introduction to A/D Conversion



only static properties are considered



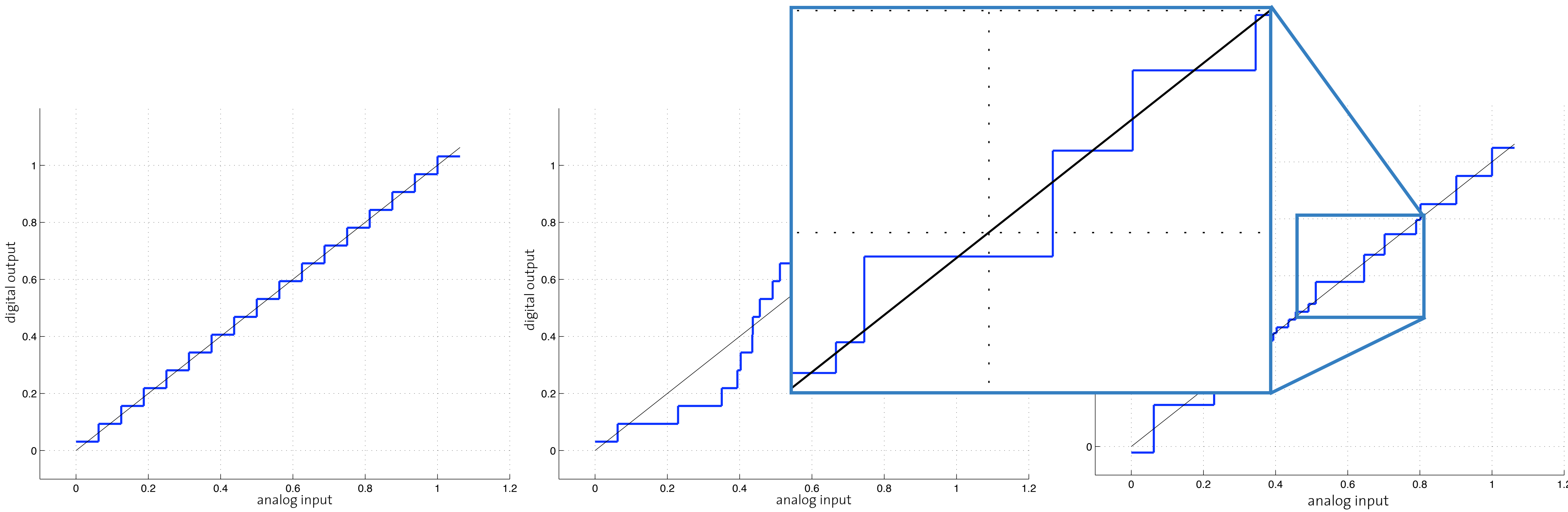
Definition: An **A/D-Converter (ADC)** converts a **continuous-amplitude**, continuous-time input signal to a **discrete-amplitude**, discrete-time signal.

Important: The threshold voltage is defined in the analog domain, the corresponding digital output is assigned and not fixed.

Maximizing the Resolution of Non-Ideal ADCs

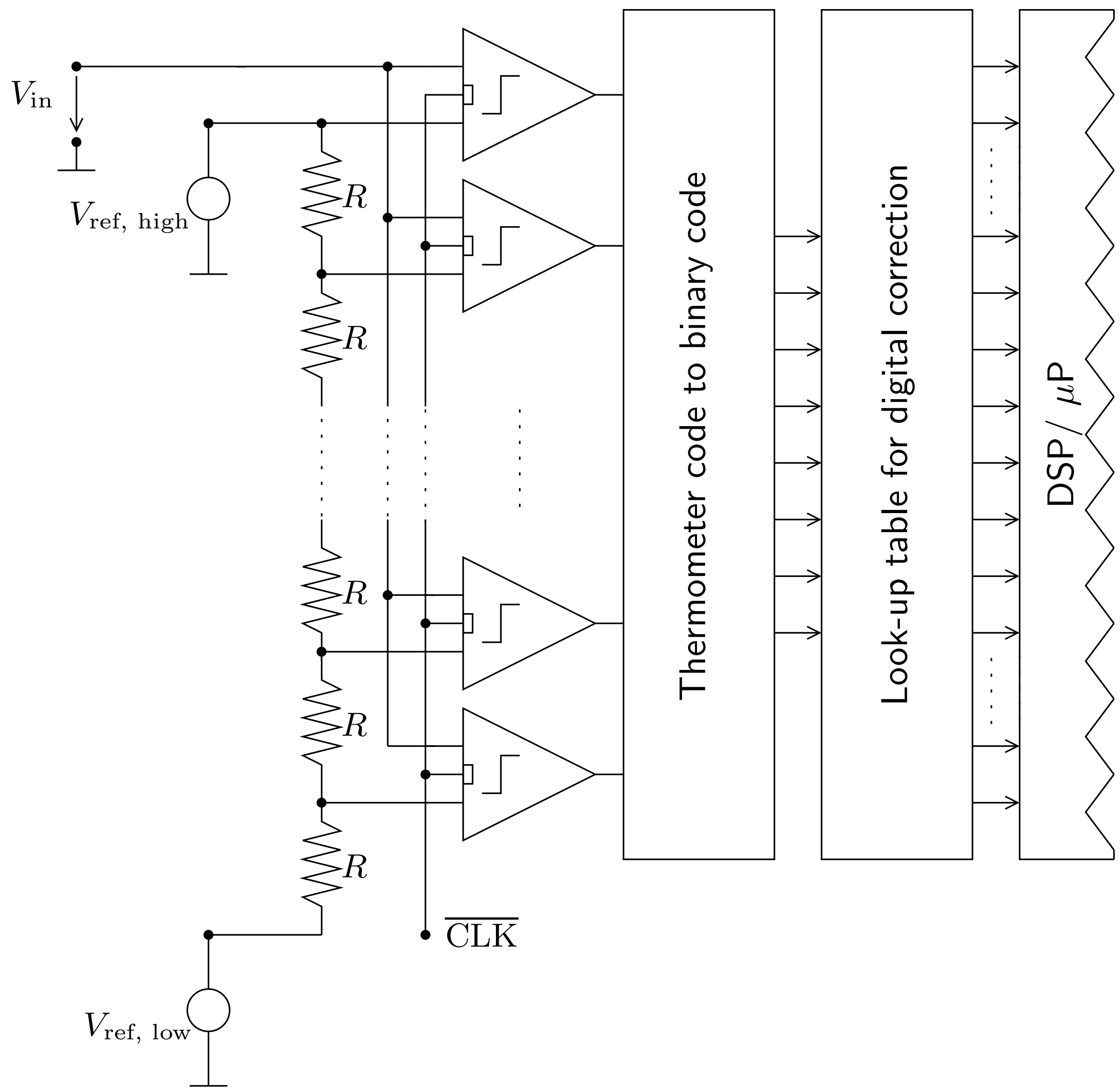
⇒ Minimizing the rms Quantization Error

Example: ideal and non-ideal 4-bit ADC



ideal 4-bit ADC	non-ideal uncorrected 4-bit ADC		non-ideal output-corrected 4-bit ADC
Q = 18.06 mV	Q = 79.25 mV		Q = 33.88 mV
Res = 4 bit	**Res = 1.87 bit**	⇒	**Res = 3.09 bit**

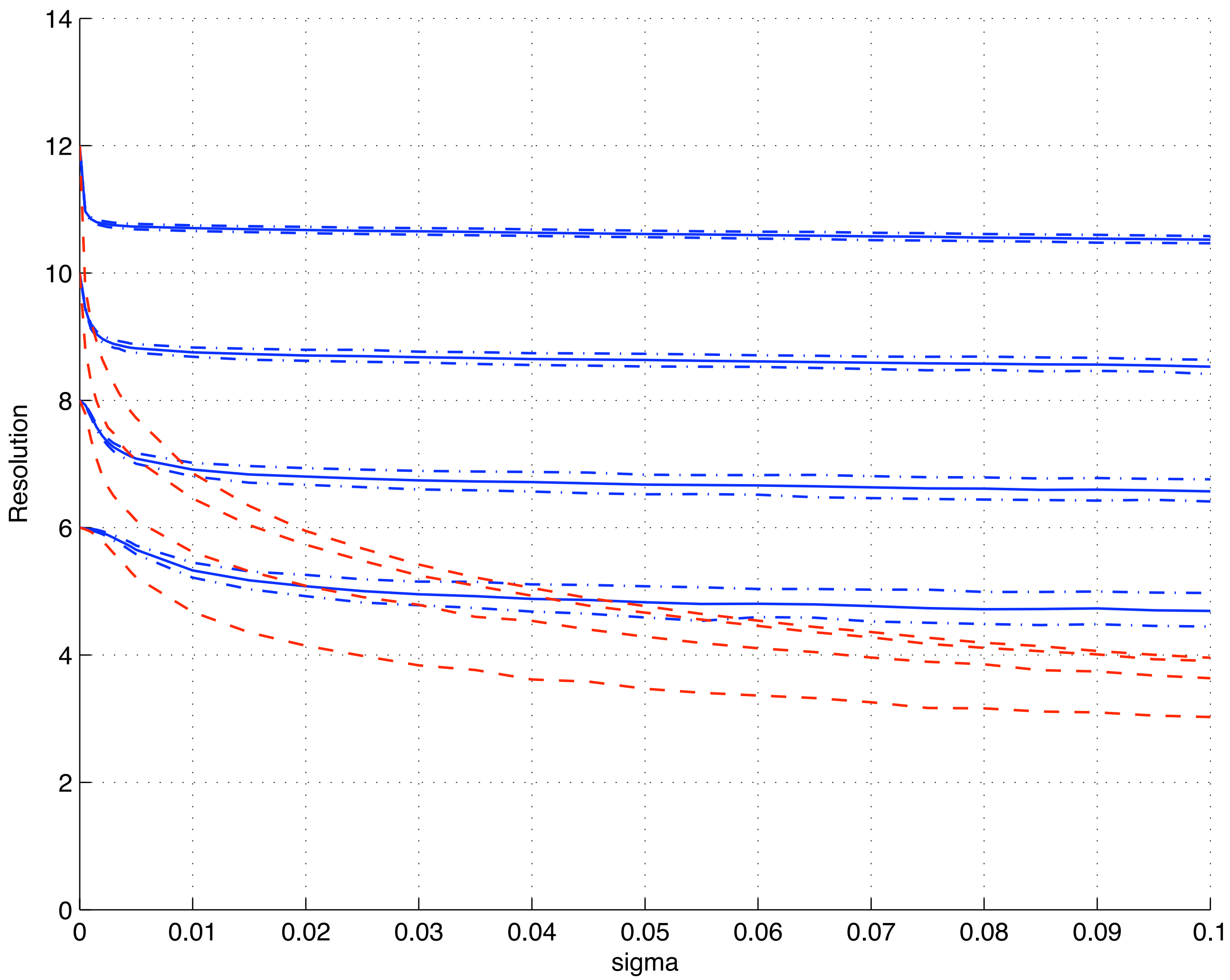
System Overview for Digitally Corrected ADCs



Digital correction tries to minimize the rms quantization error

The output of the LUT can be of higher bit-order than the effective ADC-resolution (similar to Sigma-Delta-ADCs).

Comparator-Mismatch vs. effective Resolution



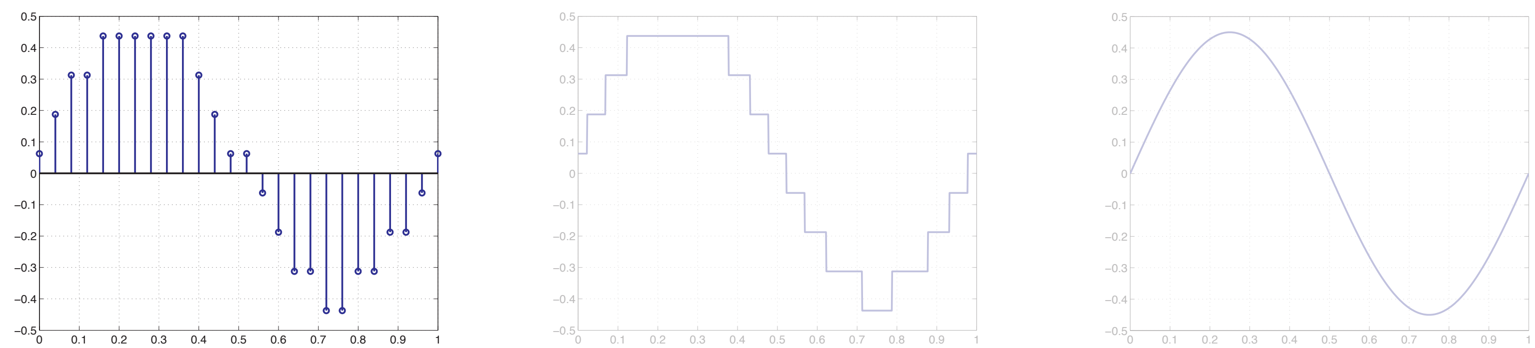
Simulation for 6-bit to 12-bit ADC's with variable comparator mismatch

➪ **The effective resolution is only weakly dependent on the comparator mismatch (applying output correction)!**

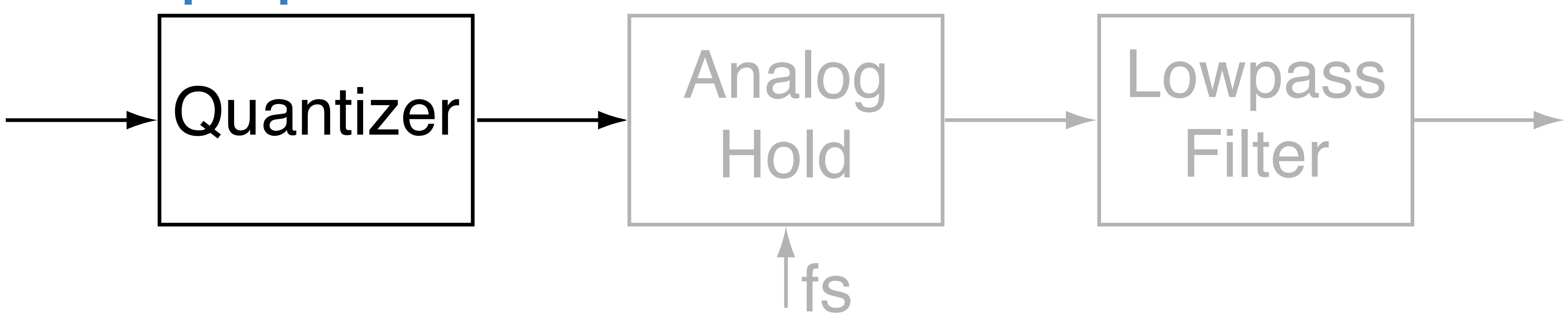
➪ **With 2^N low-precision comparators, an ADC with $Res_{eff} \approx (N\text{-}1)$ bits can be achieved.**

Introduction to D/A Conversion

0	0	1	0	1	1
1	0	1	0	0	1
0	0	1	0	1	0



only static properties are considered

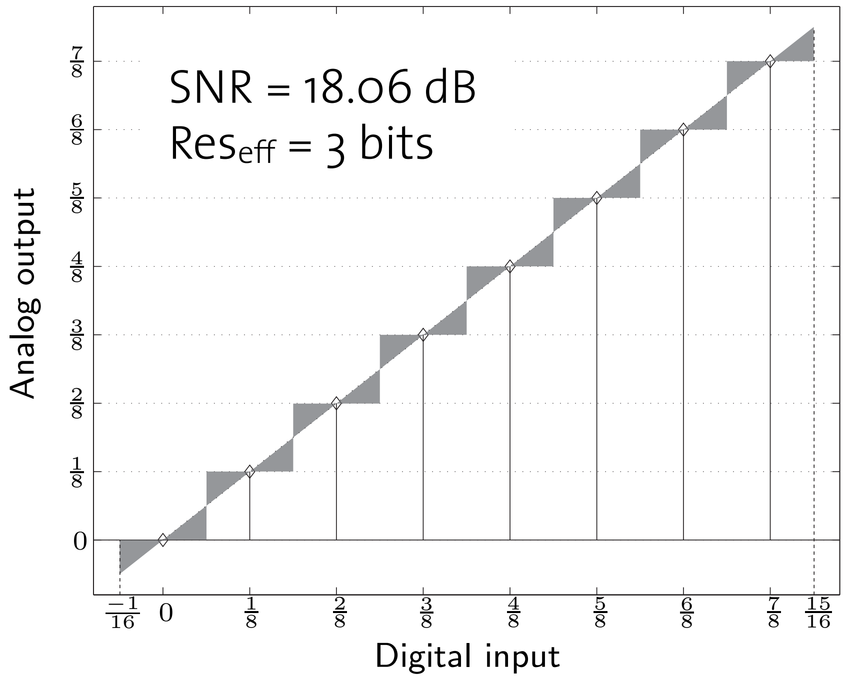


Definition: A D/A-Converter produces an **analog output *A*** that is **proportional** to a **digital input *D***: $A = \alpha D$

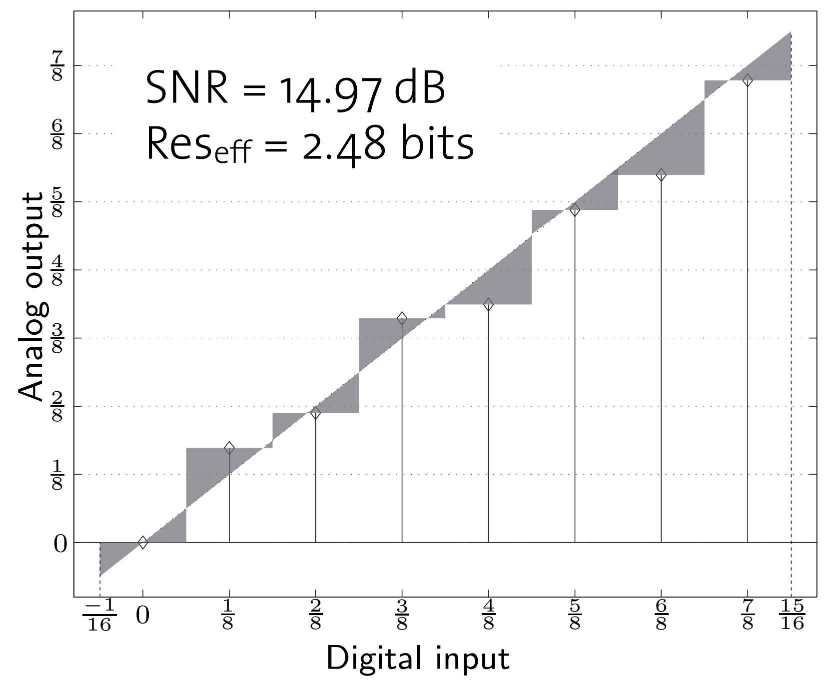
Important: The set of possible analog outputs is fixed, but the assignment from the digital inputs to the analog outputs can be adjusted.

Minimizing the rms Quantization Error in Non-Ideal DACs

Example: ideal and non-ideal 3-bit DAC

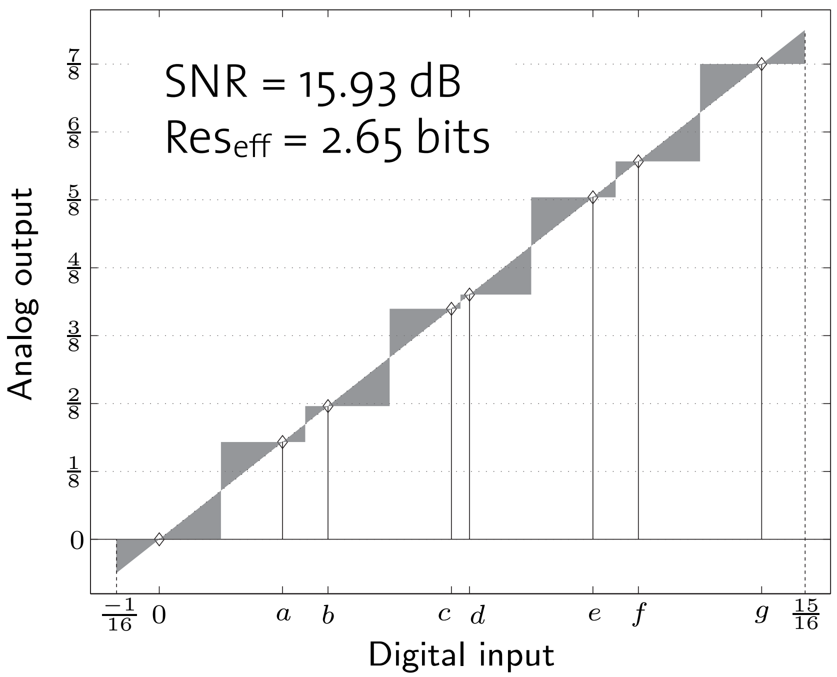


ideal 3-bit DAC
SNR = 18.06 dB
Res = 3 bit



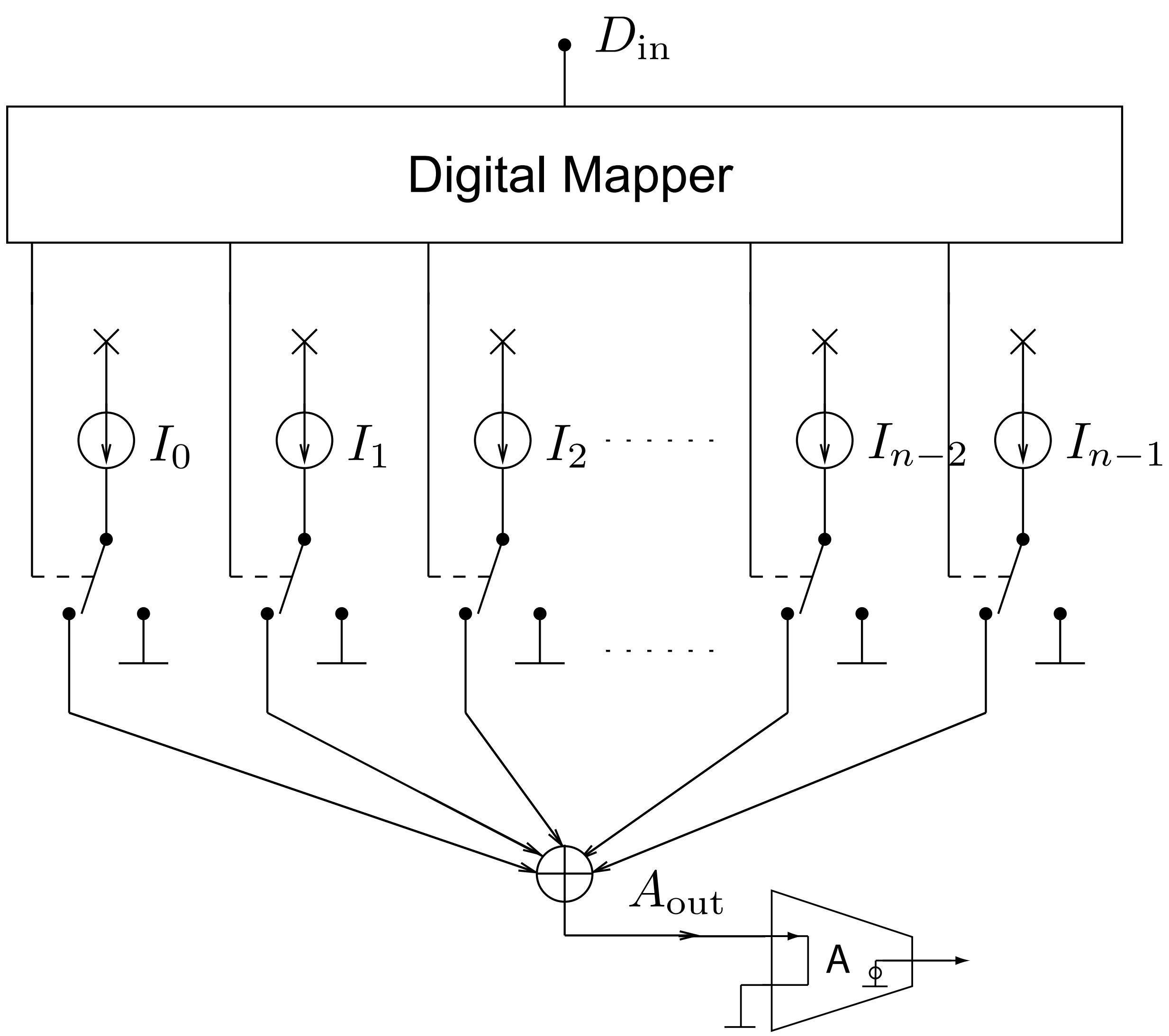
non-ideal uncorrected
3-bit DAC
SNR = 14.97 dB
Res = 2.48 bit

⇨



non-ideal input-corrected
3-bit DAC
SNR = 15.93 dB
Res = 2.65 bit

System Overview for Digitally Corrected DACs

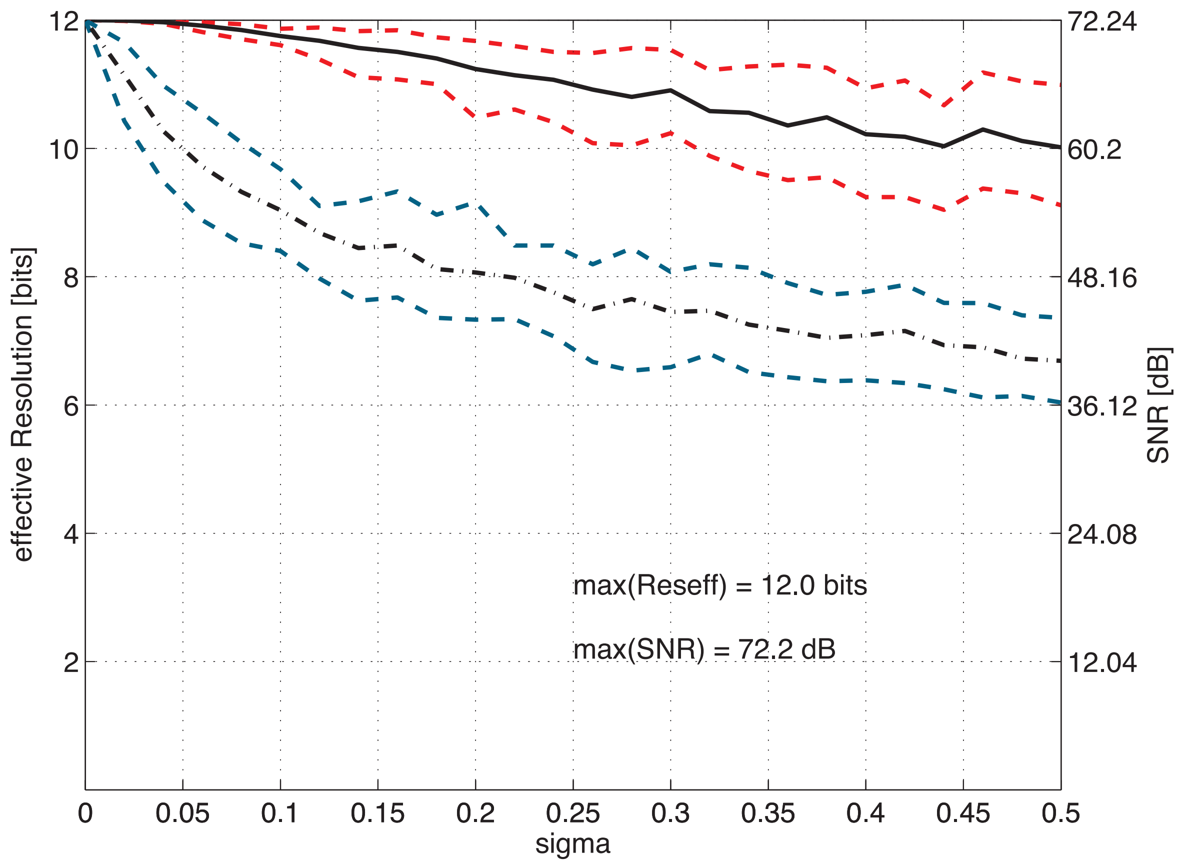


Procedure:

1. Determine the set of all 2^n possible outputs.
2. For every D_{in}, find the closest analog output (from the set of all outputs).
3. Store the switch positions leading to this analog output in a LUT.

Digitally Corrected DACs: Simulation results

12 binary-scaled current-sources with variable mismatch



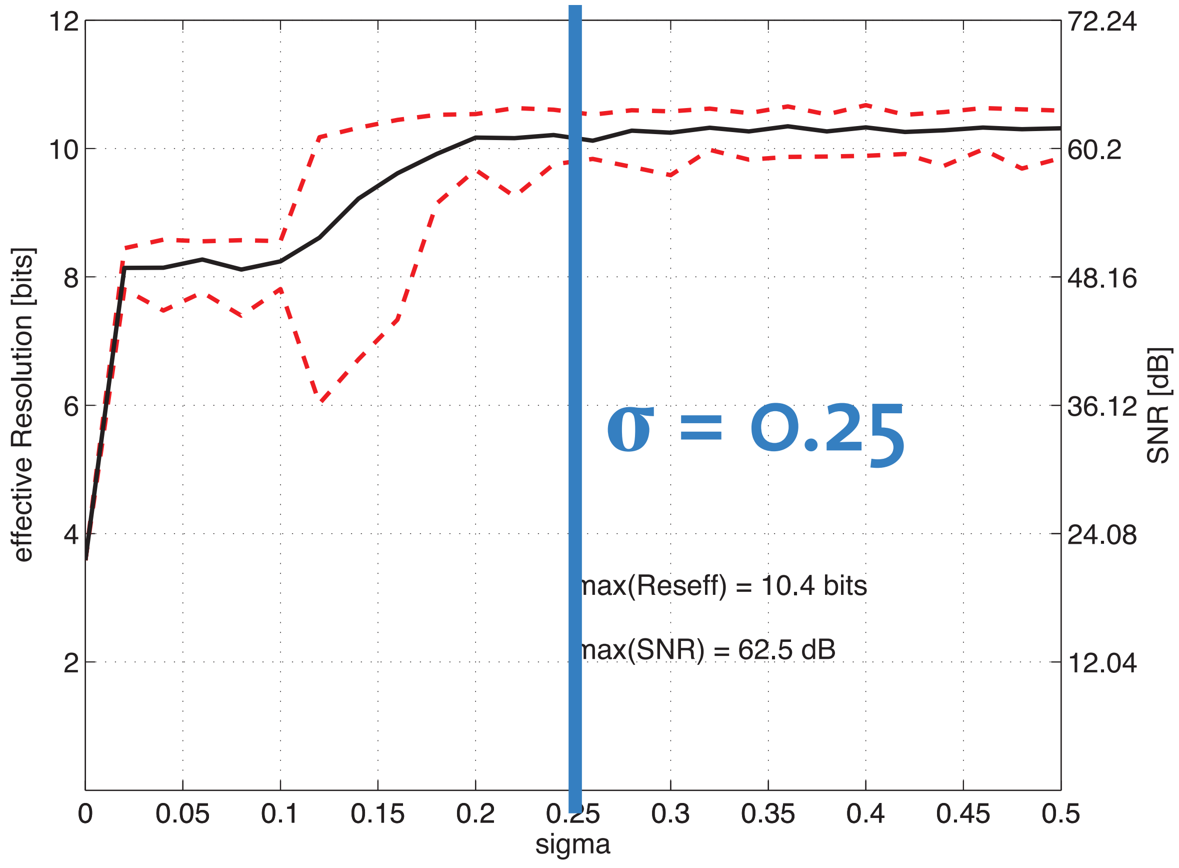
nominal size of current-sources:
1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048

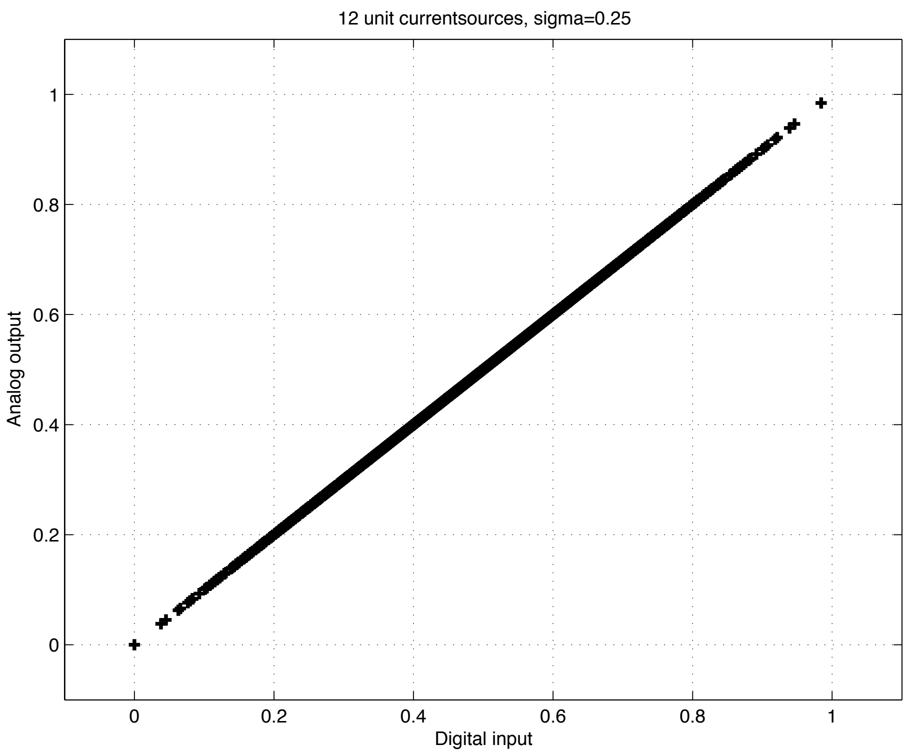
nominal area:
Σ = 4095

⇒ **Effective Resolution decreases with increased mismatch.**

Digitally Corrected DACs: Simulation results

12 unit current-sources with variable mismatch

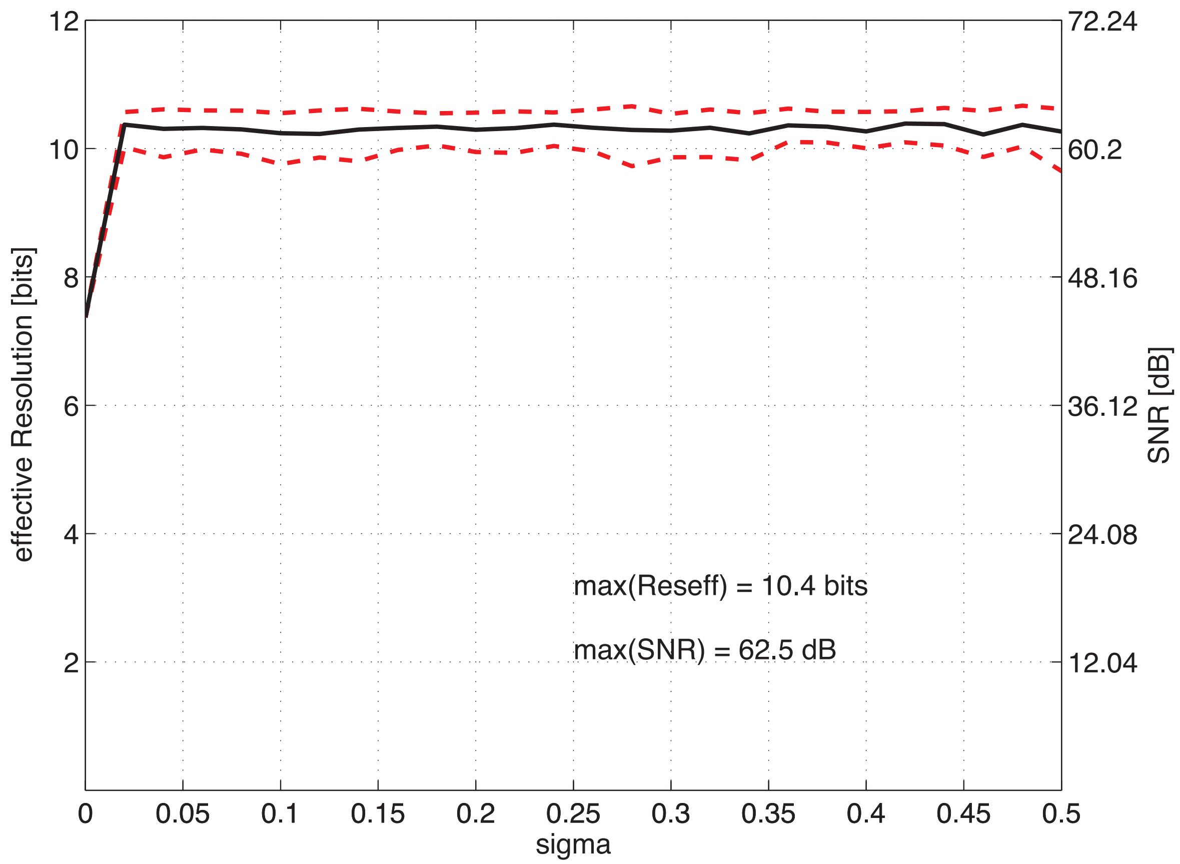




⇒ **Effective Resolution increases with increased mismatch.**

Digitally Corrected DACs: Simulation results

12 arithmetically-scaled current-sources with variable mismatch



nominal size of current-sources:
1.0, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9, 2.0, 2.1

nominal area:
$\Sigma = 18.6$

⇒ Effective Resolution increases with increased mismatch (but is nearly constant).

Conclusions, Outlook

- We presented a way to build converters with low-precision elements:
  - With **2^N minimum-sized comparators**, a flash **ADC** with an effective resolution of approximately **N-1 bits** can be achieved.
  - With **N nearly minimum-sized** current-sources, a **DAC** with an effective resolution of **N-2 bits** can be obtained.
- Outlook:
  - Practical online (and offline) on-chip calibration
  - Similar approach for Successive-Approximation ADCs

Contributions

Acknowledgments:
Patrik Strebel (all measurements)
Patrick Merkli (analog decoders)
Daniel Furrer (analog coprocessor)

- Analog Decoding & Related Topics
  - Measurements on discrete analog Hamming decoders
  - Integrated analog decoders for
    - (8,4,4) extended Hamming Code
    - (16,5,8) Reed-Muller Code
    - Coprocessor for decoding a UMTS Turbo Code
  - Soft Symbol Detection Circuit for PAM, QAM, and related schemes
- Digitally Corrected Converters
  - Integrated flash ADC for static measurements
  - Insight: Resolution of digitally corrected ADCs and DACs is (nearly) independent of mismatch